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EXAMINER	
AMRANY, ADI	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,931	THEILER, HELMUT	
	Examiner	Art Unit	
	ADI AMRANY	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed February 26, 2008 have been fully considered but they are not persuasive. Applicant's "loads" are not defined in any way to distinguish over those presented in Jain. Since the Jain switches (108, 116) receive power from the circuit array, they fall into the broad category of "loads." Further, in an alternative embodiment of Jain's figure 1, it is clear that the capacitor (124) is another load, which when combined with load 126, meets the broad limitation of "loads."

A load is defined as a device that receives power (Encarta Online Dictionary, definition #8; http://encarta.msn.com/encnet/features/dictionary/DictionaryResults.aspx?refid=1861699182). There is no recitation in applicant's claims that the loads receive current. Regardless, transistors have leakage currents between the terminals. The gate of a transistor requires at least some current to change the doping of the substrate to switch the transistor between on/off states.

Lastly, the switches (108, 116) operate with the signals (110, 122), not with the input AC power (102). The signals (110, 122) are a "rectified AC voltage." Figure 4 clearly shows that the Vgs1 and Vgs2 are "rectified," as they have no negative components.

Drawings

2. The drawings were received on February 26, 2008. These drawings are acceptable and will be entered.

Claim Objections

3. Claim 1 is objected to because there is no basis for the limitation of "load control signals" (last two lines). Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-3, 5 and 20 are rejected under 35 U.S.C. 102(a) as being anticipated by Jain (US 6,577,517).

With respect to claim 1, Jain discloses a circuit array for controlling operation of two loads (108, 116) that operate with a rectified AC voltage (fig 3; col. 2-3), the circuit array comprising:

a semiconductor switch (320) on a circuit path that includes the two loads (connected to outputs 110, 122); and a control unit (302-320) to generate a switch control signal (312) that controls the switch; wherein the control unit comprises:

a phase detection device (306) to detect whether a phase of the AC voltage is positive or negative and to output a detection signal (A1, B1) that is based on whether the phase is positive or negative; and

a logic unit (310, 320) to generate the switch control signal based on load control signals (324) and the detection signal (308).

With respect to claim 2, Jain discloses the control unit comprises a time control circuit (feedback) for generating one of the load control signals (324) at a predetermined time.

With respect to claim 3, Jain discloses the control unit comprises a sensor circuit (feedback) for generating one of the load control signals (324) in response to a sensed condition. The predetermined time for generating the load control signal of claim 2 is interpreted as the time of detecting the sensed condition of claim 3.

With respect to claim 5, Jain discloses the circuit array is part of an IC (col. 2, lines 7-8).

With respect to claim 20, Jain discloses applying a voltage to a first or second one of the loads when the AC phase is positive or negative, respectively, as discussed below in the rejection of claim 6.

6. Claims 1 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Nui (US 4,300,032).

Nui discloses a circuit array (fig 1, item 101; fig 4; col. 3-4) for controlling operation of two loads (fig 4, items 11, 36; col. 4, lines 27-35) that operate with a rectified AC voltage (output of 8; col. 3, line 33-38), comprising:

a semiconductor switch (35) coupled between the two loads and ground; and

a control unit (9, 10) to generate a switch control signal, comprising:

a phase detection device (10; col. 2, lines 31-36, col. 3, lines 33-38, line 45 to col. 4, line 9); and

a logic unit (9; col. 2, lines 31-36, col. 3, lines 33-38, line 45 to col. 4, line 35) to generate the switch control signal based on load control signals (col. 4, lines 6-9) and the detection signal.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4, 6-11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain.

With respect to claim 4, Jain discloses that the logic unit inputs multiple signals (312, 324) to produce the switching signal for the PWM. It would be obvious to one skilled in the art that the Jain logic unit comprises a multiplexer, since it is known in the art to use a multiplexer to reduce the number of transmission lines in a circuit. Jain discloses that the logic unit combines the load control signals (324) and the detection signal (312) in order to determine when to output the switch control signal (fig 4; col. 2, lines 64-67).

With respect to claim 6, Jain discloses an electronic device (fig 3; col. 2-3) comprising:

an input having leads to receive AC voltage (102);

a circuit array for controlling a switch (320) to apply voltage to two loads (110, 122) based on whether a phase of the AC voltage is positive or negative (312) and a load control signal (324);

a rectifier that is connected to the input and that provides the voltage to the loads (inherent, col. 1, lines 11-16), the voltage being generated from the AC voltage, wherein the rectifier comprises an open bridge circuit, and wherein the voltage comprises different half waves of the AC voltage that are applied to different loads (col. 2, lines 53-60).

At the time of the invention by applicant, it would have been obvious to one skilled in the art to provide a second feedback signal, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (CCPA 1977).

With respect to claims 7-11, Jain discloses the recited limitations, as discussed above in the rejections of claims 1-5, respectively.

With respect to claim 19, it would be obvious to one skilled in the art that the Jain switch is a MOSFET device, as FETs and BJTs are the most common types of transistors. Further, Jain discloses that the remaining switches in the circuit are all FETs. Lastly, discovering an optimum value of a result effective variable (type of transistor) involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADI AMRANY whose telephone number is (571)272-0415. The examiner can normally be reached on Mon-Thurs, from 10am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

AA